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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TRAN, DENISE

ART UNIT	PAPER NUMBER
2186	10

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/122,349	HACKING ET AL.	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2001 and 31 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12 and 38-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12 and 38-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 and 8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL ACTION

1. In response to the applicant's requests during the telecommunication on 03/08/01, claims 13-37 have been rejoined as new claims 42-64, the restriction requirement made in Paper No. 3 is hereby withdrawn.

2. Claims 1-12 and 38-64 are presented for examination. Claims 3 and 13-37 have been canceled.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 and 38-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rahman et al., U.S. patent No. 5,778,431, (hereinafter Rahman) in view of Tabak, RISC Systems, Research Studies Press, 1990, hereinafter Tabak.

As per claims 1, 7, 38, 42, 46, 51, 56 and 62-63, Rahman teaches the invention substantially as claimed, comprising: a first storage area to store data (e.g., fig. 1, el. 114); a cache memory having a plurality of cache lines, each of which stores data (e.g., fig.1, el. 106 and col. 5, line 27 and et seq.); a second storage area to store instructions

(e.g., col. 7, line 22 and et seq.); and an execution unit coupled to the first storage area, the second storage area, and the cache memory to operate on data elements identifying a user-definable or physical address (e.g. col. 3, lines 25-30, col. 5, lines 30-35 and col. 7, lines 25-28) to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving an instruction (e.g., col. 7, line 22 and et seq.) or copy data in a predetermined portion of the plurality of cache lines to the first storage area in response to receiving an instruction (e.g., col. 7, line 22 and et seq.); or a processor comprising a circuit to obtain a starting address of a predetermined area of the cache memory (e.g., fig.1, els. 101 or 102) by reading a portion of an address in a register specified in the code (e.g. col. 7, lines 24-28) and invalidate data in the predetermined area of cache memory (e.g., col. 7, line 22 and et seq.) or copy data from the predetermined are of cache memory and store the copy data in the storage area separate from the cache memory (e.g., col. 7, line 22 and et seq.) and a portion of a starting address of the cache line in which data to be invalidated or copied (i.e., tag address; e.g., col. 7, line 22 and et seq.). Even though Rahman teaches the use of validation being implemented through instruction and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand. Official Notice is taken that both the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its

operand to Rahman's system because it would instruct the system to do work by using data it its operand and thereby, increase controlling of the system. Rahman does not specifically show the use of decoder to decode instructions. Official Notice is taken that both the concept and advantages of providing a decoder to decode an instruction are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction. Rahman does not specifically show the use of the single processor instruction being of a processor instruction. Rahman does however show the use of the microprocessor as example having a CPU core with RISC operations (e.g. col. 5, lines 5-12). Rahman is not clear on whether or not the microcode referenced previously is one of the RISC operations. Tabak shows the use of a one-to-one correspondence between the RISC operations and the microcode (e.g. page 9, third paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Tabak with Rahman because it would provide for fast and efficient processing of instructions as a hardwired control, and still let the designer benefit from the advantages of microprogramming, as taught by Tabak (same paragraph).

As per claims 2, 4, 6, 8-9, 11-12, 39, 41, 43, 45, 47, 49-50, 52, 55, 57, 60-61, and 64, Rahman shows a register address values (i.e., a memory register address; e.g., col.7); a portion of a starting address of the cache line in which data to be invalidated or copied (i.e., tag address; e.g., col. 7, line 22 and et seq.); the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag

address; e.g., col. 7, line 22 and et seq.); the predetermined portion of the plurality of cache lines is a page in the cache memory (i.e., a page can be a cache line; e.g., col.7); an execution unit coupled to the first storage area, the second storage area, and the cache memory to operate on data elements to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving an instruction (e.g., col. 7, line 22 and et seq.) or copy data in a predetermined portion of the plurality of cache lines to the first storage area in response to receiving an instruction (e.g., col. 7, line 22 and et seq.); and setting an invalid bit corresponding to the predetermined area of cache memory (e.g., col. 5, line 40 and et seq.) . Even though Rahman teaches the use of validation being implemented through instruction and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand. Official Notice is taken that both the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would instruct the system to do work by using data it its operand and thereby, increase controlling of the system. Rahman does not specifically show the use of decoder to decode instructions. Official Notice is taken that both the concept and advantages of providing a decoder to decode an instruction are well known and expected in the art. It would have been obvious to one of ordinary skill

in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction.

As per claims 5, 10, 40, 44, 48, 53-54, 58-59, Rahman shows the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag address; e.g., col. 7, line 22 and et seq.); Rahman does not specifically show execution unit shifts the data elements or portion of an address by a predetermined number of bits positions represent a number of least significant bits to obtain the starting address of the cache line in which data to be invalidated or copied. Even though Rahman teaches the use of validation being implemented through instruction and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand. Official Notice is taken that both the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would instruct the system to do work by using data it its operand and thereby, increase controlling of the system. Rahman does not specifically show the use of decoder to decode instructions. Official Notice is taken that both the concept and advantages of providing a decoder to decode an instruction are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address

values of an instruction. Official Notice is taken that both the concept and advantages of shifting the data elements or portion of an address by a predetermined number of bits positions are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have shifting the data elements by a predetermined number of bits positions to Rahman's system because it would allow rearrange an order of address bits in a particular sequence.

5. Applicants remarks filed 6/19/01, not deemed moot in view of the new grounds of rejection necessitated by Applicant's amendment, have been considered but are not persuasive.

6. In the remarks, Applicants argue in substance that Rahman does not teach or suggest that the portion of the starting address to include a plurality of most significant bits of the starting address as disclosed by claims 4, 9, 15, 20, 27 and 32.

The examiner respectfully disagrees as cited in the previous office action, Rahman shows the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag address; e.g., col. 7, line 22 and et seq.).

7. Because Applicant has failed to properly or seasonably challenge the examiner's Official Notices in the previous office action, those limitations are now considered as prior art. MPEP 2144.03.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday, and an alternate Wed. from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7467-239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DT

D.T.
July 18, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100